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(54) INTERFERENCE SIGNAL ELIMINATOR

(57) Matched filters 102-1 to 102-n extract channel estimated values corresponding to users 1 to n by finding correlation with the reception signal. Threshold processing sections 103-1 to 103-n perform threshold processing on estimated power values obtained based on the channel estimated values corresponding to users 1 to n. JD section 104 performs matrix calculations using channel estimated values subjected to threshold processing. Multiplication section 105 performs a multiplication between the matrix calculation result and the reception signal. Identifier 106 performs hard decision on the multiplication result.

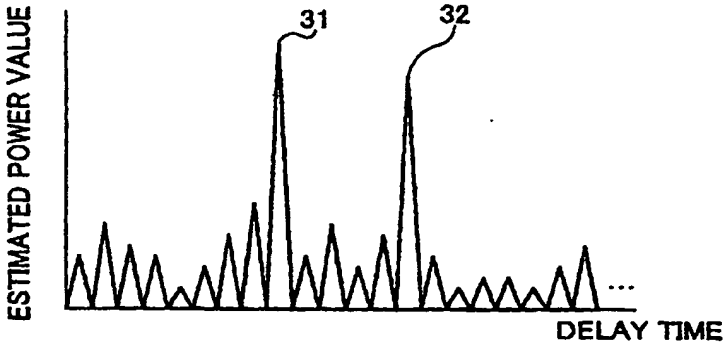

FIG.3

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Description

Technical Field

[0001] The present invention relates to a CDMA (Code Division Multiple Access)-based communication apparatus, and more particularly, to an interference signal eliminator that eliminates interference using matrix calculations.

Background Art

[0002] One of conventional methods for eliminating various interference such as interference due to multi-path fading, inter-symbol interference and multiple-access interference, and extracting a demodulated signal is an interference signal elimination method using Joint Detection (hereinafter referred to as "JD"). This JD is disclosed in "Zero Forcing and Minimum Mean-Square-Error Equalization for Multiuser Detection in Code-Division Multiple-Access Channels" (Klein A., Kaleh G.K., Baier P.W., IEEE Trans. Vehicular Technology, vol.45, pp.276-287, 1996).

[0003] An apparatus for implementing the conventional interference signal elimination method using JD will be explained using FIG.1 and FIG.2 below. In the following explanation, the number of users to be demodulated is assumed to be n.

[0004] FIG.1 is a block diagram showing a conFguration of a conventional interference signal eliminator using JD. FIG.2 is a schematic diagram showing a frame format used in the conventional interference signal eliminator using JD.

[0005] In FIG.1, a reception signal is sent to delayer 11 and matched Hters 12-1 to 12-n. Here, the reception signal above has been received by an antenna (not shown in the Fgure) and subjected to predetermined processing such as frequency conversion by a radio section (not shown in the Fgure). In delayer 11, the reception signal is delayed by a predetermined time and sent to multiplication section 14 which will be described later.

[0006] In matched Hters 12-1 to 12-n, channel estimation is performed for each user using a midamble section (see FIG.2) in a time slot of the reception signal. That is, in matched Hters 12-1 to 12-n, a channel estimated value (matrix) for each user is obtained by Fnding a correlation between known midambles assigned to users 1 to n and the midamble section of the reception signal above within a maximum estimated delay range. Then, the channel estimated value for each of users 1 to n is sent from matched Hters 12-1 to 12-n to Joint Detection (hereinafter referred to as "JD") section 13.

[0007] JD section 13 performs the following matrix calculations using the channel estimated value for each user above. That is, a convolution calculation is performed between the channel estimated value for each user and a spreading code assigned to each user and a convolution calculation result (matrix) for each user is thereby obtained.

[0008] In this way, a matrix made up of regularly placed convolution calculation results of their respective users (hereinafter referred to as "system matrix") is obtained. Here, for brevity of explanation, the system matrix is expressed as [A]. Furthermore, the following matrix [B] is obtained by performing a matrix calculation shown in the following expression using the system matrix:

$$[B] = ([A]^{H} \cdot [A])^{-1} \cdot [A]^{H} \qquad ①$$

where, $[A]^H$ is a conjugate transposed matrix of the system matrix and $([A]^H \cdot [A])^{-1}$ is an inverse matrix of $[A]^H \cdot [A]$.

[0009] The matrix [B] obtained from the above matrix calculation is sent to multiplication section 14. In multiplication section 14, data for each user free of interference is obtained by carrying out multiplication processing between the data section (see FIG.2) of the reception signal sent from delayer 11 and the matrix sent from JD section 13. The data for each user obtained at this time is sent to identiFer 15. IdentiFer 15 performs hard decision on the data for each user sent from multiplication section 14 and demodulated data is obtained.

[0010] As shown above, the conventional interference signal eliminator using JD obtains demodulated data with interference eliminated without performing despreading or RAKE combining.

[0011] However, the conventional interference signal eliminator using JD has a problem of including not a little possibility that the accuracy of demodulated data will reduce for the reasons described below.

[0012] First, the channel estimated values obtained for respective users by matched Hters 12-1 to 12-n have the potential for including errors, and therefore the matrix calculation results obtained by JD section 13 also have the potential for including errors. As a result, the accuracy of demodulated data obtained from multiplication section 14 may deteriorate.

[0013] Here, errors included in the channel estimated values will be explained with reference to FIG.3. FIG.3 is a schematic diagram showing a delay proHe of a user obtained by channel estimation in the conventional interference

signal eliminator using JD.

[0014] As shown in FIG.3, from a channel estimated value estimated using a matched filter, a user's path and delay time of the path are obtained. That is, valid paths 31 and 32 with high estimated power are obtained and delay times of the valid paths are also obtained.

[0015] In this way, channel estimation is performed for each user. However, the channel estimation results sent to JD section 13 are not only the above mentioned valid paths but include other errors, and therefore the accuracy of the matrix calculation results obtained from JD section 13 deteriorates.

[0016] Secondly, in a CDMA-based communication, it is desirable to reduce transmit power of the apparatus on the transmitting side to a necessary minimum in order to suppress interference with other users. Therefore, when there is no data to be sent during a call, a method of sending only the midamble section in the aforementioned time slot (see FIG.2) is adopted. This method is called "DTX."

[0017] In the case where a user (here, suppose user 2) only sends a midamble using DTX, since the conventional interference signal eliminator using JD receives the midamble section from user 2, it recognizes that the data section is also received from user 2. As a result, JD section 13 performs the aforementioned matrix calculations with the understanding that it is receiving the data section from user 2.

[0018] However, since user 2 is not sending the data section, the demodulated data resulting from a multiplication between the matrix calculation result from JD section 13 and reception signal includes an error. Moreover, trying to demodulate an originally non-existent signal of user 2 may cause an abnormal operation of the entire equipment.

[0019] As described above, the conventional interference signal eliminator using JD has a problem of including the potential for reducing the accuracy of demodulated data obtained.

Disclosure of Invention

[0020] The present invention has been implemented taking account of the problems described above and it is an object of the present invention to provide an interference signal eliminator capable of extracting demodulated data with high accuracy.

[0021] This object will be attained by applying threshold decision to an estimated power value calculated based on the channel estimated value obtained from the reception signal and applying the threshold decision result to matrix calculations.

Brief Description of Drawings

[0022]

FIG.1 is a block diagram showing a configuration of a conventional interference signal eliminator using JD;

FIG.2 is a schematic diagram showing a frame format used by the conventional interference signal eliminator using JD;

FIG.3 is a schematic diagram showing a delay profile obtained by channel estimation by the conventional interference signal eliminator using JD;

FIG.4 is a block diagram showing a configuration of an interference signal eliminator according to Embodiment 1 of the present invention;

FIG. 5 is a schematic diagram showing a delay profile obtained by power calculation on a channel estimated value in the interference signal eliminator according to Embodiment 1;

FIG.6 is a schematic diagram showing a delay profile obtained by threshold processing in the interference signal eliminator according to Embodiment 1;

FIG.7 is a graph showing the accuracy of demodulated data obtained by the interference signal eliminator according to Embodiment 1; and

FIG.8 is a block diagram showing a configuration of an interference signal eliminator according to Embodiment 2 of the present invention.

Best Mode for Carrying out the Invention

[0023] With reference now to the attached drawings, embodiments of the present invention will be explained in detail below.

(Embodiment 1)

[0024] FIG.4 is a block diagram showing a configuration of an interference signal eliminator according to Embodi-

ment 1 of the present invention. In the following explanations, the number of users is assumed to be n.

[0025] In FIG.4, delayer 101 sends a reception signal delayed by a predetermined time to multiplication section 105 which will be described later. Matched filters 102-1 to 102-n extract channel estimated values for their respective users 1 to n by finding a correlation using the reception signal and send the extracted channel estimated values to threshold processing sections 103-1 to 103-n.

[0026] Threshold processing sections 103-1 to 103-n perform threshold processing on estimated power obtained based on channel estimated values for their respective users 1 to n and send the threshold processing results to Joint Detection (hereinafter referred to as "JD") section 104. Details of the threshold processing of threshold processing sections 103-1 to 103-n will be given later.

[0027] JD section 104 performs matrix calculations using channel estimated values sent from threshold processing sections 103-1 to 103-n and sends the matrix calculation results to multiplication section 105. Multiplication section 105 multiplies the matrix calculation result from JD section 104 by the reception signal from delayer 101 and sends the multiplication result to identifier 106.

[0028] Identifier 106 performs hard decision on the multiplication result from multiplication section 105 and extracts demodulated data.

[0029] Then, the operation of the interference signal eliminator with the above configuration will be explained. The reception signal is the signal that is sent with the time slot shown in FIG.2, received via an antenna (not shown in the figure) and subjected to predetermined processing such as frequency conversion by a reception section (not shown in the figure). The time slot shown in FIG.2 is the same as that described above and therefore detailed explanations will be omitted.

[0030] First, the above reception signal is sent to delayer 101 and matched filters 102-1 to 102-n. At delayer 101, the reception signal is delayed by a predetermined time and sent to multiplication section 105.

[0031] Matched filters 102-1 to 102-n use the midamble section (see FIG.1) in the time slot of the reception signal and perform channel estimation for each user. That is, matched filters 102-1 to 102-n find a correlation between known midambles assigned to users 1 to n and the midamble section in the above reception signal within a maximum estimated delay range and obtain a channel estimated value (matrix) for each user. Here, the above channel estimated value is expressed in a complex number made up of an I component and Q component.

[0032] Then, matched filters 102-1 to 102-n send the channel estimated values for users 1 to n to threshold processing sections 103-1 to 103-n, respectively.

[0033] Threshold processing sections 103-1 to 103-n performs threshold processing on estimated power obtained by applying power calculation on the channel estimated values of users 1 to n sent from their respective matched filters 102-1 to 102-n. Here, for brevity, the threshold processing of each threshold processing section will be explained below taking threshold processing 103-1 that handles a channel estimated value of user 1 as an example and with reference to FIG.5 and FIG.6.

[0034] FIG.5 is a schematic diagram showing a delay profile obtained by power calculation on a channel estimated value of matched filter 102-1 in the interference signal eliminator according to Embodiment 1 of the present invention. FIG.6 is a schematic diagram showing a delay profile of user 1 obtained by threshold processing of threshold processing section 103-1 in the interference signal eliminator according to Embodiment 1 of the present invention.

[0035] FIG.5 shows the magnitude of channel estimated power at intervals over time. Here, estimated power is calculated by power calculation on a channel estimated value, that is, by finding the sum of the squares of the I component and Q component of the channel estimated value.

[0036] First, of all estimated power values, power values whose magnitude is greater than a threshold are decided to be valid paths and power values whose magnitude is smaller than the threshold are decided to be invalid paths. As a result, path 201 and path 202 are decided to be valid paths, while the other estimated power values are decided to be invalid paths. Here, these invalid paths are paths of users other than user 1 or power of estimated values produced by various other factors. In this way, the only valid paths are path 201 and path 202 as shown in FIG.6.

[0037] Then, in a channel estimated value, parts other than the valid paths (chip unit) are eliminated and the elimination result is sent to JD section 104 as channel estimated values after threshold processing of user 1.

[0038] The above threshold is set as follows. That is, an appropriate threshold is obtained based on the accuracy of demodulated data obtained through a plurality of demodulation processes and a threshold set each time. Thus, it is possible to set a value obtained by subtracting X[dB] from the maximum estimated power value as the optimal threshold.

[0039] Moreover, aside from the above method, it is also possible to extract a threshold with optimal accuracy of demodulated data from among thresholds obtained by a plurality of demodulation processes and set an average of this threshold as an optimal threshold. By the way, the threshold can be changed as appropriate not only by the method above but also according to various conditions such as the accuracy of the demodulated data and conditions of the transmission path.

[0040] Furthermore, it is also possible to increase/decrease the optimal threshold set above according to various

conditions and use it as a new threshold. This is what the threshold processing is all about.

[0041] The channel estimated values after threshold processing by threshold processing sections 103-1 to 103-n are sent to JD section 104.

[0042] JD section 104 performs the following matrix calculations using the channel estimated value for each user. That is, by carrying out convolution calculation between the channel estimated value for each user and spreading code assigned to each user, a convolution calculation result (matrix) for each user is obtained.

[0043] From this, a matrix with the convolution calculation results of users regularly placed (hereinafter referred to as "system matrix") is obtained. For brevity of explanation, the system matrix is expressed as [A] here.

[0044] Moreover, by carrying out a matrix multiplication according to the above expression ① using the system matrix, a matrix [B] is obtained.

[0045] The matrix [B] obtained by the above matrix calculation is sent to multiplication section 105. Multiplication section 105 performs multiplication processing between the data section of the reception signal sent from delayer 101 (see FIG.1) and a matrix sent from JD section 104 and in this way data for each user free of interference is obtained. The data for each user obtained at this time is sent to identifier 105. Identifier 105 performs hard decision on the data for each user sent from multiplication section 104 and thereby obtains demodulated data.

[0046] Then, the accuracy of demodulated data obtained from the interference signal eliminator of this embodiment will be explained with reference to FIG.7. FIG.7 is a graph that shows the accuracy of demodulated data obtained by the interference signal eliminator of this embodiment in comparison with the accuracy of the conventional apparatus.

[0047] FIG.7 shows BER (bit error rate) of demodulated data versus the ratio of noise power density of the reception signal ("NO" in the figure) to average code energy per one bit of the reception signal ("Eb" in the figure) in both the interference signal eliminator of this embodiment and the conventional interference signal eliminator. In the figure, the ○ plots denote values measured by the interference signal eliminator of this embodiment and the △ plots denote values measured by the conventional interference signal eliminator.

[0048] As is clear from the figure, this embodiment can suppress transmit power necessary to maintain BER of demodulated data at a certain level to a level lower than the conventional system. That is, the interference signal eliminator of this embodiment can not only improve the accuracy of demodulated data but also suppress transmit power at the apparatus on the transmitting side without influencing the accuracy of demodulated data. This can suppress interference with other users.

[0049] As shown above, this embodiment performs matrix calculation using the result of eliminating the part corresponding to invalid paths in channel estimated values and then extracts demodulated data using this matrix calculation result, and therefore can obtain high accuracy demodulated data. This embodiment can also reduce transmit power of the apparatus on the transmitting side, and therefore can suppress interference with other users.

(Embodiment 2)

[0050] Embodiment 2 is a mode that allows Embodiment 1 to handle signals sent using DTX. The interference signal eliminator according to this embodiment will be explained with reference to FIG.8 below.

[0051] FIG.8 is a block diagram showing a configuration of the interference signal eliminator according to Embodiment 2 of the present invention. The parts in FIG.8 with the same configuration as that of Embodiment 1 (FIG.4) will be assigned the same reference numerals as those in FIG.4 and their detailed explanations will be omitted. Regarding the interference signal eliminator according to Embodiment 2, only the parts different from those of Embodiment 1 will be explained below.

[0052] The apparatus on the transmitting side transmits a signal containing information on DTX to the interference signal eliminator according to this embodiment beforehand. That is, the apparatus on the transmitting side transmits a signal with information indicating whether DTX is used or not, in other words, information on whether only the midamble section is sent or the entire signal including the data section is sent, added to the midamble section of the above time slot (see FIG.2).

[0053] As described above, the interference signal eliminator according to this embodiment receives the signal sent from the apparatus on the transmitting side.

[0054] In FIG.8, the channel estimated values obtained by matched filters 102-1 to 102-n are sent to switches 301-1 to 301-n and control section 500 through paths, which are not shown in the figure.

[0055] Control section 500 uses the channel estimation results from matched filters 102-1 to 102-n to decide whether each signal is sent by each user using DTX or not. Furthermore, control section 500 sends signals about switching control to switches 301-1 to 301-n according to the above decision result.

[0056] That is, to those of switches 301-1 to 301-n whose corresponding user signal is sent using DTX, control section 500 sends a signal informing that a channel estimated value will be sent to the reset section, whereas to those switches whose corresponding user signal is sent without using DTX, control section 500 sends a signal informing that a channel estimated value will be sent to the threshold processing section as in the case of Embodiment 1.

[0057] Switches 301-1 to 301-n send the channel estimated values sent from the matched filters 102-1 to 102-n to reset sections 302-1 to 302-n or threshold processing sections 103-1 to 103-n according to the control signal from control section 500 above.

[0058] In reset sections 302-1 to 302-n, channel estimated values sent from switches 301-1 to 301-n are reset. The reset results are sent to JD section 104. This reset result is equivalent to the output result in this case where there are no users.

[0059] In JD section 104, the user signal sent using DTX is treated as a signal of a non-existent user and the above described matrix calculation is performed. As a result, high accuracy demodulated data is obtained from identifier 106.

[0060] Thus, this embodiment resets a channel estimated value corresponding to the user whose data section does not exist in the reception signal according to information on DTX contained in the midamble section in the reception signal, making it possible to perform accurate matrix calculations. This allows high accuracy demodulated data to be extracted.

[0061] The interference signal eliminator explained in the above embodiments can be mounted on a base station apparatus and radio communication terminal apparatus in a CDMA-based radio communication system.

[0062] As described above, the present invention can provide an interference signal eliminator capable of extracting demodulated data with high accuracy.

[0063] The interference signal eliminator of the present invention adopts a configuration comprising a matched filter calculation section that performs correlation processing between reception signals from a plurality of other ends of communication and a known signal and calculates a channel estimated value, a threshold decision section that performs threshold decision on an estimated power value obtained from the channel estimated value and a joint detection calculation section that performs a joint detection calculation on the threshold decision result and obtains demodulated data.

[0064] This configuration allows parts corresponding to invalid paths of the channel estimated value to be eliminated by comparing estimated power calculated based on the channel estimated value obtained from the reception signals with a threshold, making it possible to extract demodulated data with high accuracy.

[0065] The interference signal eliminator of the present invention adopts a configuration comprising an extraction section that extracts an identification signal indicating the presence/absence of data from a reception signal, with the threshold decision section resetting a channel estimated value corresponding to the other end of communication of which the identification signal indicates the absence of data and sending the channel estimated value to the joint detection calculation section.

[0066] This configuration allows accurate matrix calculation processing by resetting a channel estimated value corresponding to the other end of communication including no data section, making it possible to extract demodulated data with high accuracy and prevent abnormal operations of the apparatus.

[0067] The interference signal eliminator of the present invention adopts a configuration with the threshold decision section setting a channel estimated value corresponding to an estimated power value of less than a threshold to zero and only sending a channel estimated value corresponding to an estimated power value exceeding the threshold to the joint detection calculation section.

[0068] This configuration allows the parts corresponding to invalid paths in the channel estimated value to be removed and allows matrix calculations to be performed accurately. This makes it possible to extract demodulated data with high accuracy.

[0069] The interference signal eliminator of the present invention adopts a configuration with the matched filter calculation section performing matched filter calculations only for a predetermined period in consideration of a delay of the reception signal.

[0070] This configuration allows channel estimation taking into account each user's delay time in the reception signal, thus allowing channel estimated values more accurately. This also makes it possible to extract more accurate demodulated data.

[0071] The base station apparatus of the present invention comprises an interference signal eliminator and the interference signal eliminator adopts a configuration comprising a matched filter calculation section that performs correlation processing between reception signals from a plurality of other ends of communication and a known signal and calculates a channel estimated value, a threshold decision section that performs threshold decision on the estimated power value obtained from the channel estimated value and a joint detection calculation section that performs a joint detection calculation on the threshold decision result and obtains demodulated data.

[0072] The communication terminal apparatus of the present invention performs a radio communication with a base station equipped with an interference signal eliminator and the interference signal eliminator adopts a configuration comprising a matched filter calculation section that performs correlation processing between receptions signals from a plurality of other ends of communication and a known signal and calculates a channel estimated value, a threshold decision section that performs threshold decision on the estimated power value obtained from the channel estimated value and a joint detection calculation section that performs a joint detection calculation on the threshold decision result and obtains demodulated data.

[0073] These configurations incorporate an interference signal eliminator capable of extracting demodulated data with high accuracy, providing the base station apparatus and communication terminal apparatus that implement optimal communications.

[0074] The interference signal elimination method of the present invention comprises a matched filter calculation step that performs correlation processing between reception signals from a plurality of other ends of communication and a known signal and calculates a channel estimated value, a threshold decision step that performs threshold decision on the estimated power value obtained from the channel estimated value and a joint detection calculation step that performs a joint detection calculation on the threshold decision result and obtains demodulated data.

[0075] This method allows parts corresponding to invalid paths of the channel estimated value to be eliminated by comparing estimated power calculated based on the channel estimated value obtained from the reception signals with a threshold, making it possible to extract demodulated data with high accuracy.

[0076] The interference signal elimination method of the present invention comprises an extraction step that extracts an identification signal showing the presence/absence of data from a reception signal, with the threshold decision step resetting a channel estimated value corresponding to the other end of communication of which the identification signal indicates the absence of data and sending the channel estimated value to the joint detection calculation step.

[0077] This method allows accurate matrix calculation processing by resetting a channel estimated value corresponding to the other end of communication including no data section, making it possible to extract demodulated data with high accuracy and prevent abnormal operations of the apparatus.

[0078] This application is based on the Japanese Patent Application No.HEI 11-103047 filed on March 6, 1999, entire content of which is expressly incorporated by reference herein.

Industrial Applicability

[0079] The present invention is ideally applicable to a field of CDMA (Code Division Multiple Access)-based communication apparatuses.

Claims

1. An interference signal eliminator comprising:

   matched filter calculating means for performing correlation processing between reception signals from a plurality of other ends of communication and a known signal and calculating a channel estimated value;
   threshold deciding means for performing threshold decision on an estimated power value obtained from the channel estimated value; and
   joint detection calculating means for performing a joint detection calculation on the threshold decision result and obtaining demodulated data.

2. The interference signal eliminator according to claim 1, further comprising extracting means for extracting an identification signal indicating the presence/absence of data from the reception signal, wherein the threshold deciding means resets a channel estimated value corresponding to the other end of communication of which the identification signal indicates the absence of data and sends the channel estimated value reset to the joint detection calculating means.

3. The interference signal eliminator according to claim 1, wherein the threshold deciding means sets a channel estimated value corresponding to an estimated power value of less than a threshold to zero and sends only a channel estimated value corresponding to an estimated power value exceeding the threshold to the joint detection calculating means.

4. The interference signal eliminator according to claim 1, wherein the matched filter calculating means performs matched filter calculations only for a predetermined period in consideration of a delay of the reception signal.

5. A base station apparatus equipped with an interference signal eliminator, said interference signal eliminator comprising:

   matched filter calculating means for performing correlation processing between reception signals from a plurality of other ends of communication and a known signal and calculating a channel estimated value;
   threshold deciding means for performing threshold decision on the estimated power value obtained from the channel estimated value; and

joint detection calculating means for performing a joint detection calculation on the threshold decision result and obtaining demodulated data.

6. A communication terminal apparatus that performs a radio communication with a base station equipped with an interference signal eliminator, said interference signal eliminator comprising:

matched filter calculating means for performing correlation processing between reception signals from a plurality of other ends of communication and a known signal and calculating a channel estimated value;
threshold deciding means for performing threshold decision on the estimated power value obtained from the channel estimated value; and
joint detection calculating means for performing a joint detection calculation on the threshold decision result and obtaining demodulated data.

7. An interference signal elimination method comprising:

the matched filter calculating step of performing correlation processing between reception signals from a plurality of other ends of communication and a known signal and calculating a channel estimated value;
the threshold deciding step of performing threshold decision on the estimated power value obtained from the channel estimated value; and
the joint detection calculating step of performing a joint detection calculation on the threshold decision result and obtaining demodulated data.

8. The interference signal elimination method according to claim 7, further comprising:

the extracting step of extracting an identification signal indicating the presence/absence of data from the reception signal, wherein the threshold deciding step resets a channel estimated value corresponding to the other end of communication of which the identification signal indicates the absence of data and sends the channel estimated value reset to the joint detection calculating step.

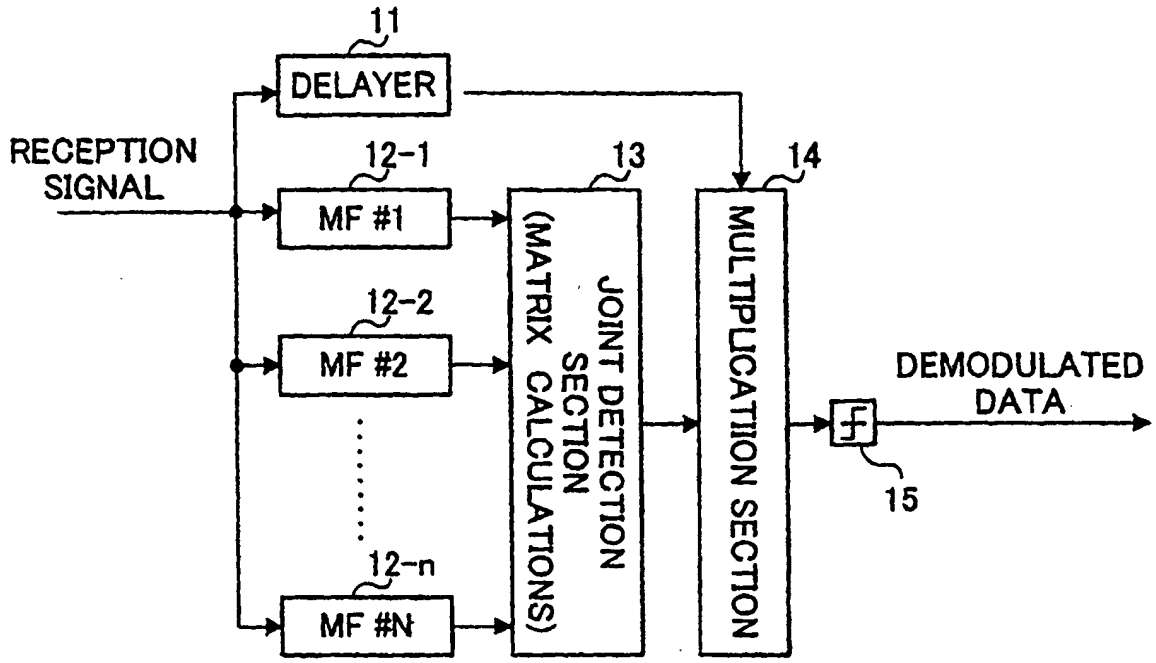
11
DELAYER
RECEPTION SIGNAL
12-1
MF #1
12-2
MF #2
12-n
MF #N
13
JOINT DETECTION SECTION (MATRIX CALCULATIONS)
14
MULTIPLICATIION SECTION
DEMODULATED DATA
15

FIG.1

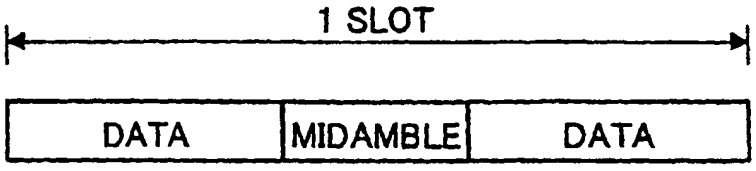
1 SLOT
DATA
MIDAMBLE
DATA

FIG.2

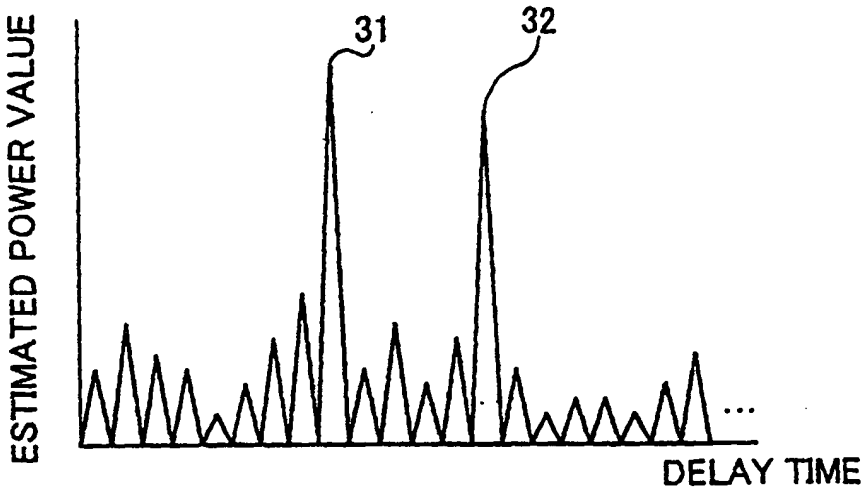

FIG.3

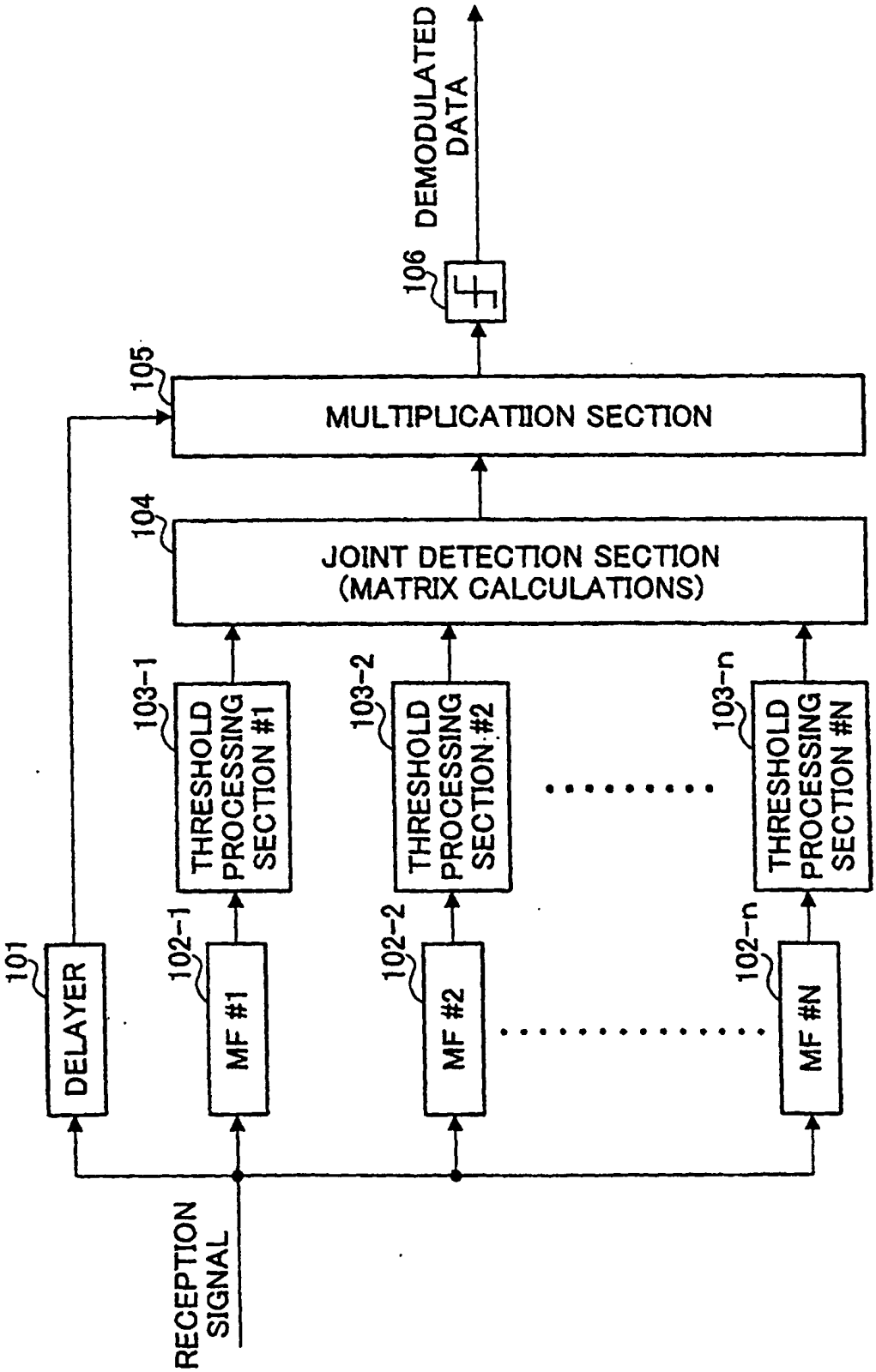
DEMODULATED DATA
106
105
MULTIPLICATIION SECTION
104
JOINT DETECTION SECTION (MATRIX CALCULATIONS)
103-1
THRESHOLD PROCESSING SECTION #1
103-2
THRESHOLD PROCESSING SECTION #2
103-n
THRESHOLD PROCESSING SECTION #N
102-1
MF #1
102-2
MF #2
102-n
MF #N
101
DELAYER
RECEPTION SIGNAL

FIG.4

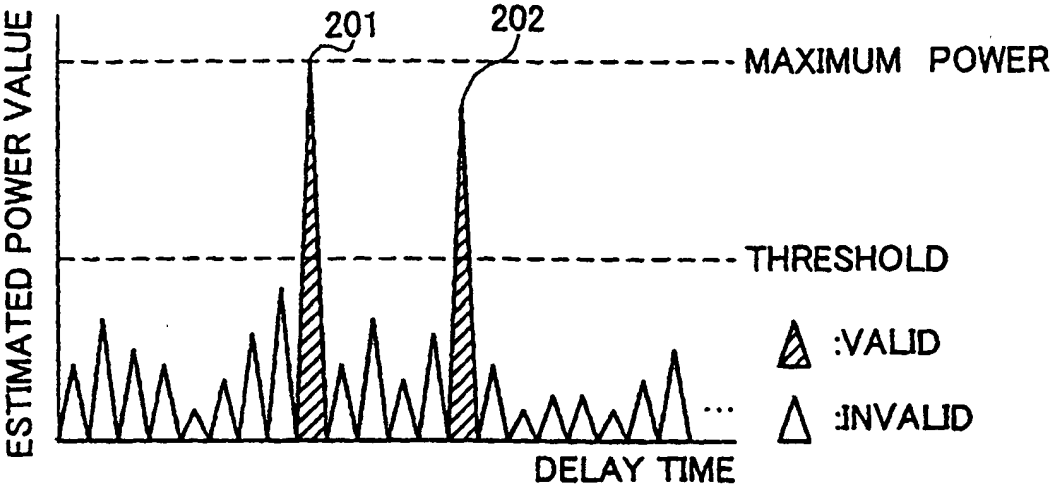
201
202
MAXIMUM POWER
THRESHOLD
ESTIMATED POWER VALUE
:VALID
:INVALID
...
DELAY TIME

FIG.5

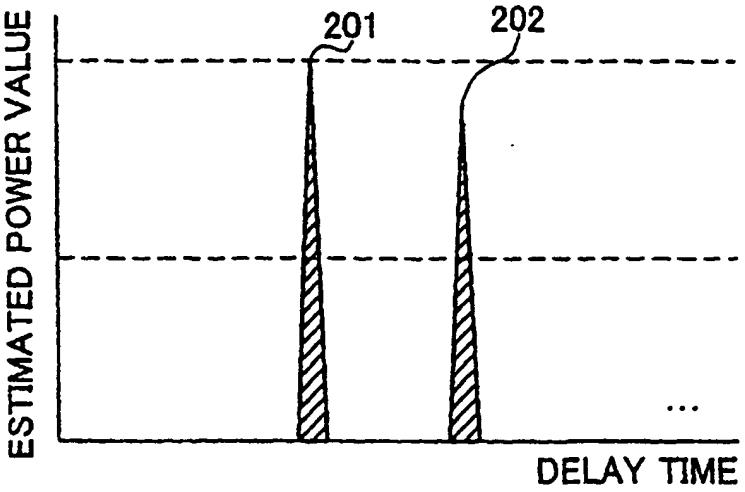
201
202
ESTIMATED POWER VALUE
...
DELAY TIME

FIG.6

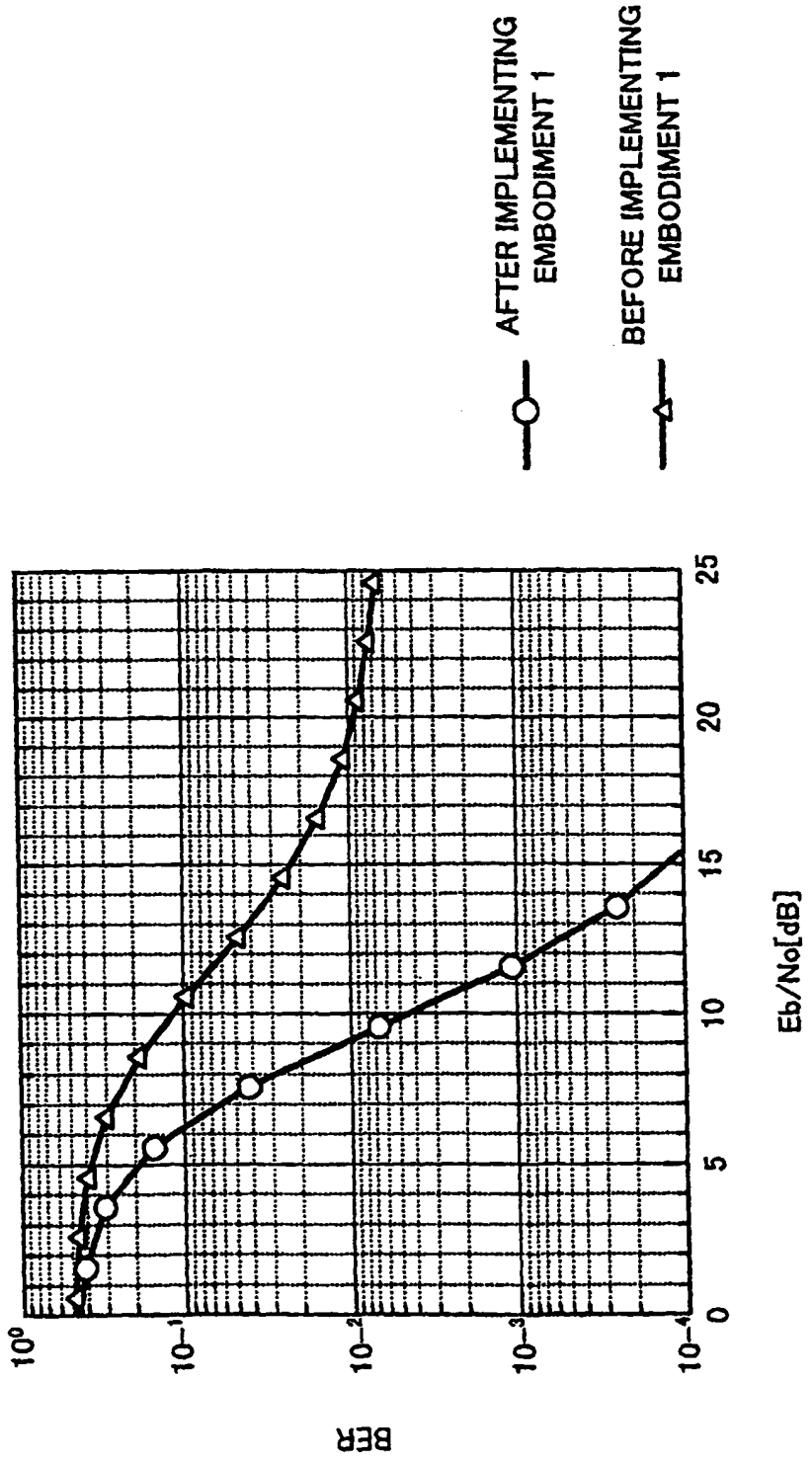
AFTER IMPLEMENTING EMBODIMENT 1
BEFORE IMPLEMENTING EMBODIMENT 1
BER
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
0
5
10
15
20
25
Eb/No[dB]

FIG.7

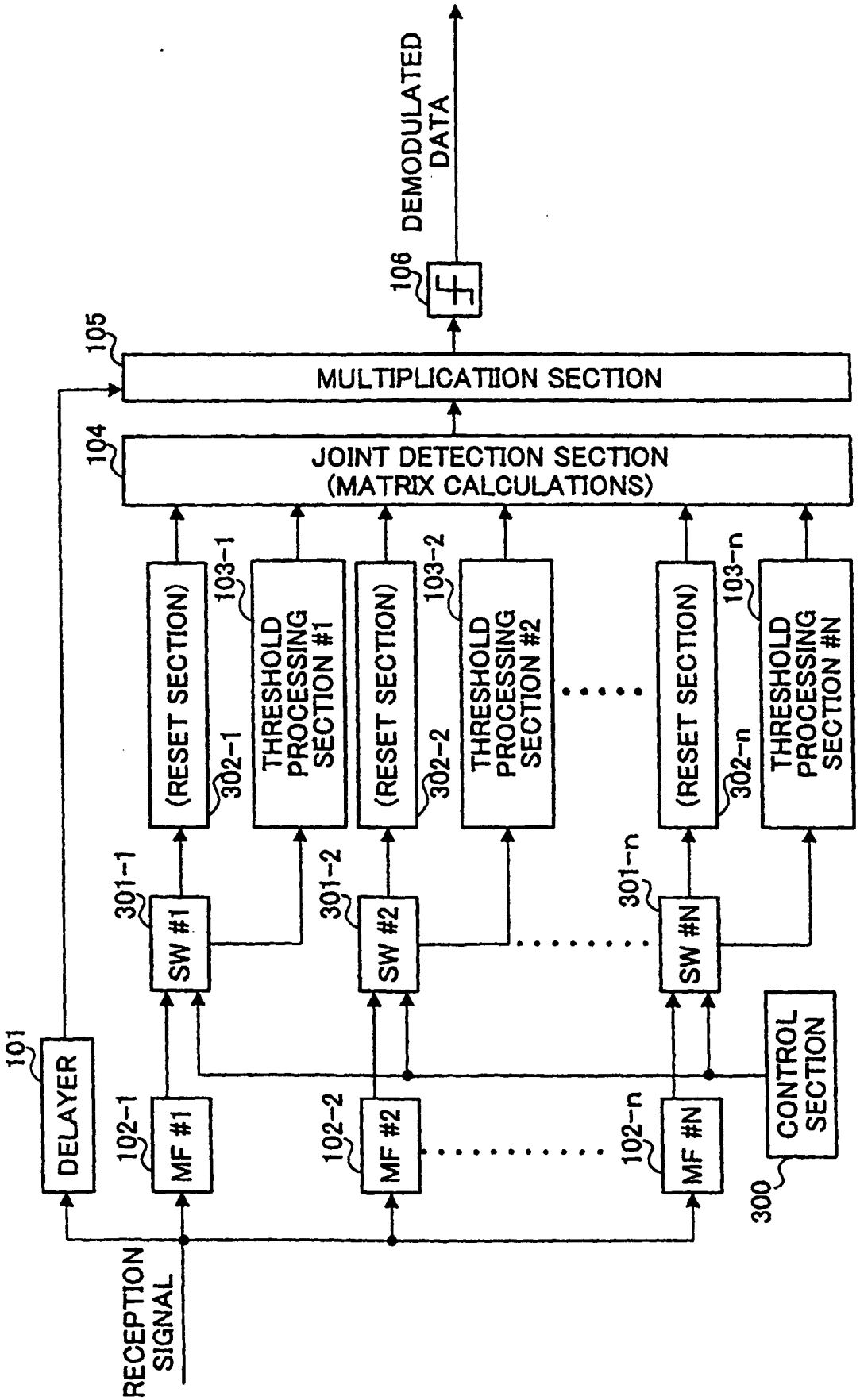
RECEPTION SIGNAL
DELAYER
101
MF #1
102-1
MF #2
102-2
MF #N
102-n
CONTROL SECTION
300
SW #1
301-1
SW #2
301-2
SW #N
301-n
(RESET SECTION)
302-1
THRESHOLD PROCESSING SECTION #1
103-1
(RESET SECTION)
302-2
THRESHOLD PROCESSING SECTION #2
103-2
(RESET SECTION)
302-n
THRESHOLD PROCESSING SECTION #N
103-n
JOINT DETECTION SECTION (MATRIX CALCULATIONS)
104
MULTIPLICATIION SECTION
105
106
DEMODULATED DATA

FIG.8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/01253

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H04J13/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H04J13/00-13/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-2000
Kokai Jitsuyo Shinan Koho 1971-2000 Jitsuyo Shinan Toroku Koho 1996-2000

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
JOIS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP, 9-200179, A (Kokusai Electric Co., Ltd.), 31 July, 1997 (31.07.97), Column 4, line 20 to Column 7, line 43; Fig. 1 & EP, 784385, A1 & US, 5956333, A	1,3-8 2
Y A	Peter Jung and Josef Blanz, "Joint Detection with Coherent Receiver Antenna Diversity in CDMA Mobile Radio Systems", IEEE Transactions on Vehicular Technology, Vol.44,No.1(02,95),p.76-88	1,3-8 2
A	JP, 6-268630, A (Kokusai Denshin Denwa Co., Ltd.(KDD)), 22 September, 1994 (22.09.94), Column 2, line 8 to Column 8, line 4; Fig. 1 (Family: none)	1-8
A	JP, 7-212274, A (Nippon Telegr. & Teleph. Corp. <NTT>), 11 August, 1995 (11.08.95), Full text; Figs. 1 to 4 (Family: none)	1-8

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 May, 2000 (30.05.00)	13.06.00
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/01253

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO, 97/33401, A1 (Kokusai Denshin Denwa Co., Ltd. (KDD)), 12 September, 1997 (12.09.97), Full text; Figs. 1 to 18 & KR, 99008345, A & SE, 9704026, A	1-8
A	JP, 10-126383, A (Matsushita Electric Ind. Co., Ltd.), 15 May, 1998 (15.05.98), Full text; Figs. 1 to 6 & US, 6002727, A	1-8
P,A	JP, 11-266184, A (Matsushita Electric Ind. Co., Ltd.), 28 September, 1999 (28.09.99), Full text; Fig. 1 (Family: none)	1-8